

FIG. 1

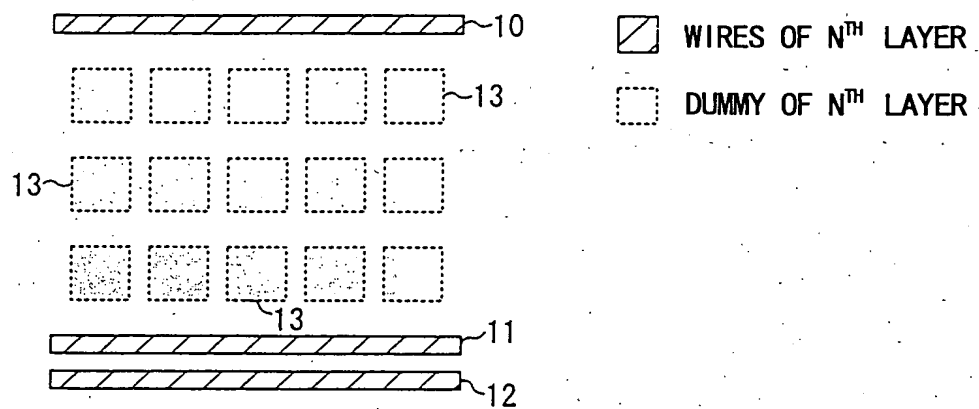


FIG. 2

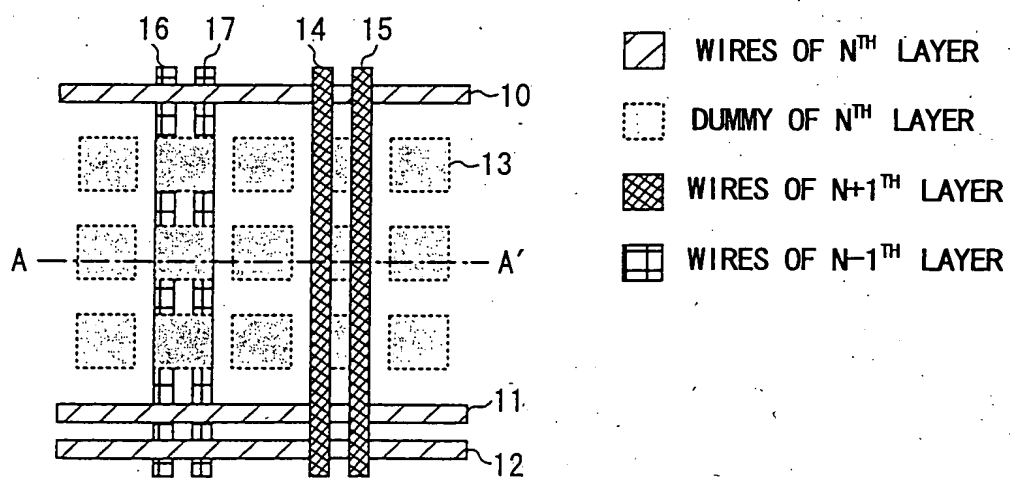


FIG. 3

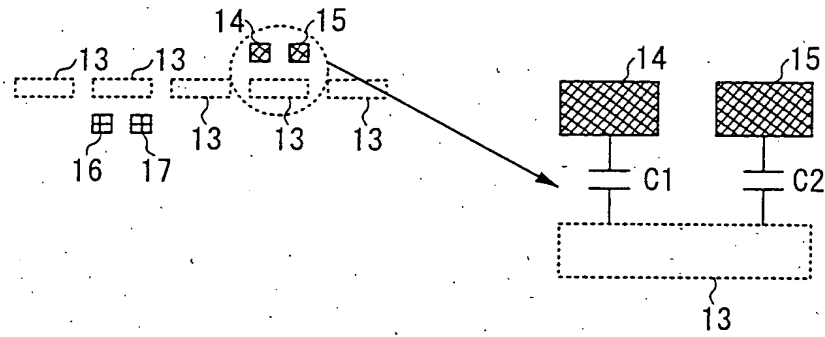
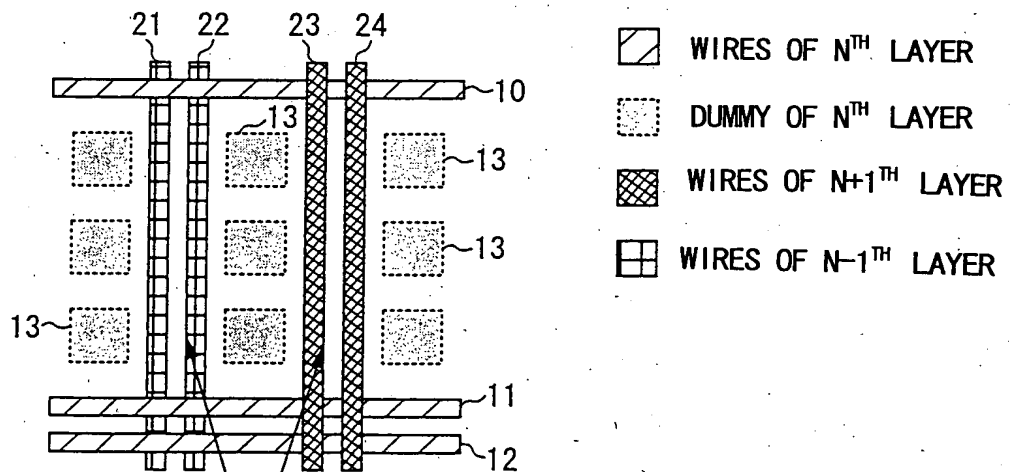


FIG. 4



NO DUMMY IN NTH LAYER OVER AND UNDER WIRES OF N+1TH LAYER AND WIRES OF N-1TH LAYER.

FIG. 5

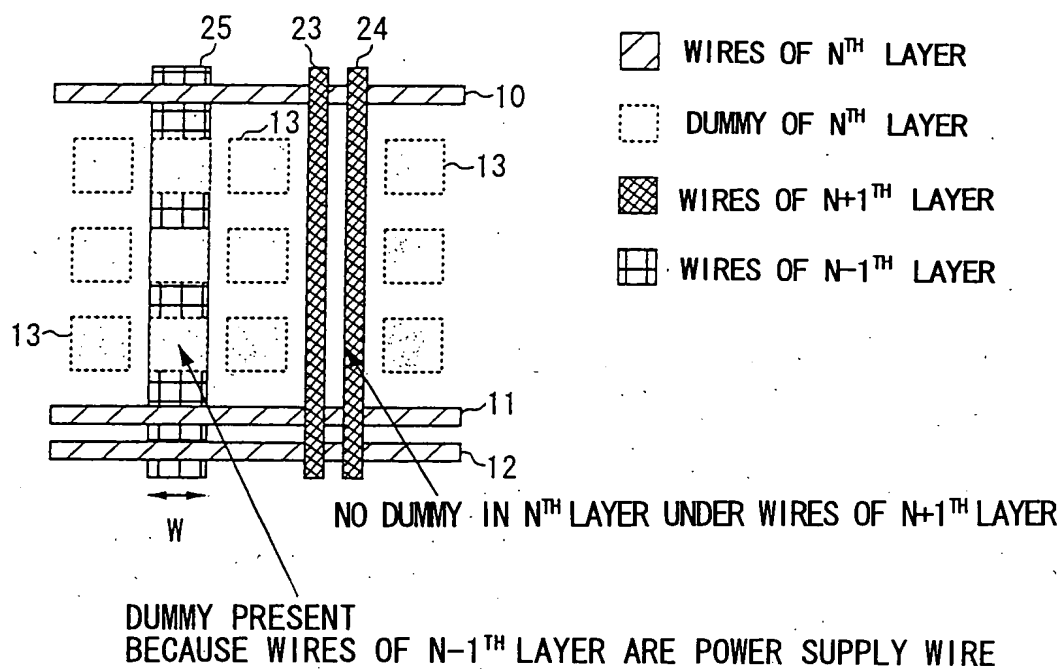


FIG. 6

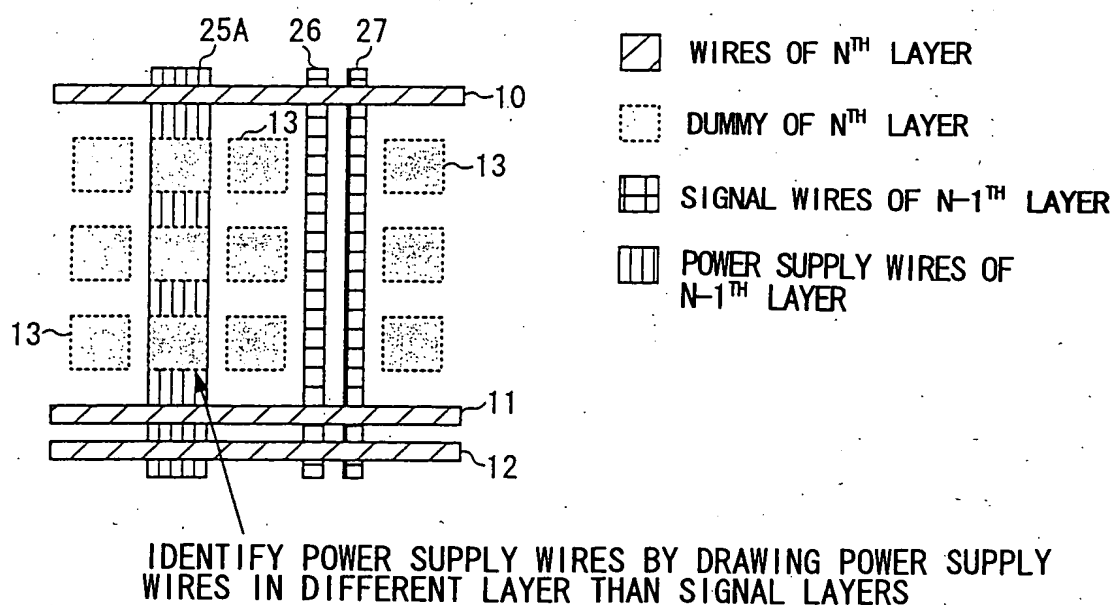
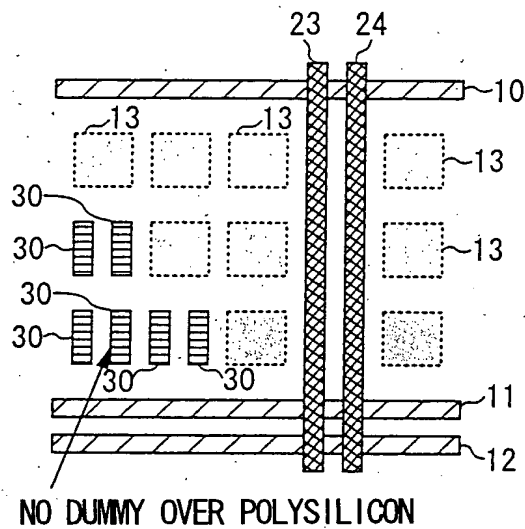


FIG. 7







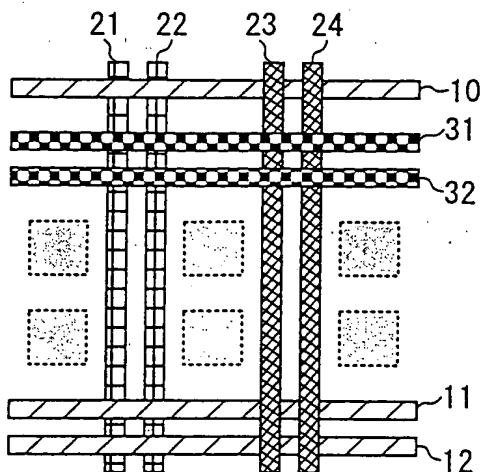





-  WIRES OF NTH LAYER
-  DUMMY OF NTH LAYER
-  WIRES OF N+1TH LAYER
-  POLYSILICON OR DIFFUSION LAYER (N-1TH LAYER)

FIG. 8



-  WIRES OF NTH LAYER
-  DUMMY OF NTH LAYER
-  WIRES OF N+1TH LAYER
-  WIRES OF N-MTH LAYER (M IS POSITIVE INTEGER)
-  WIRES OF N-1TH LAYER

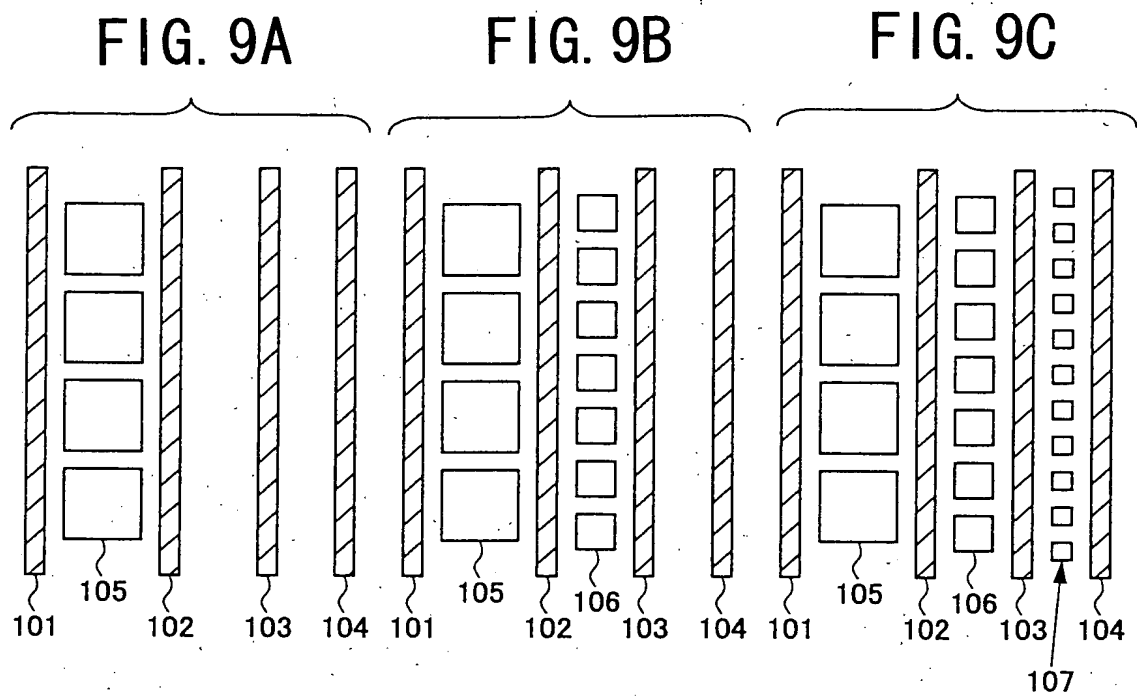


FIG. 10

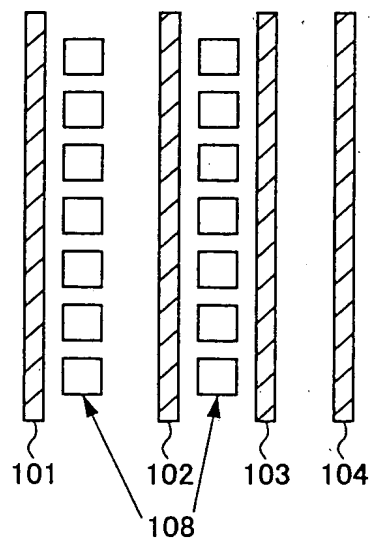


FIG. 14A

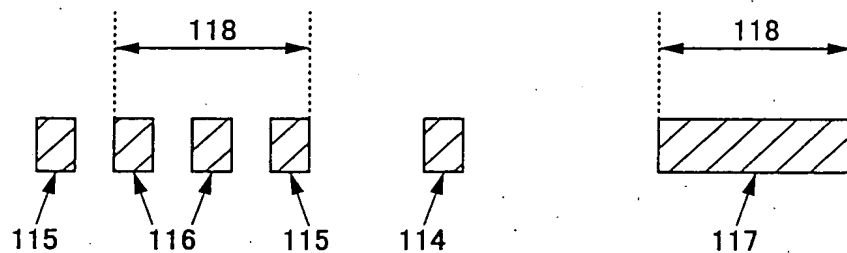


FIG. 14B

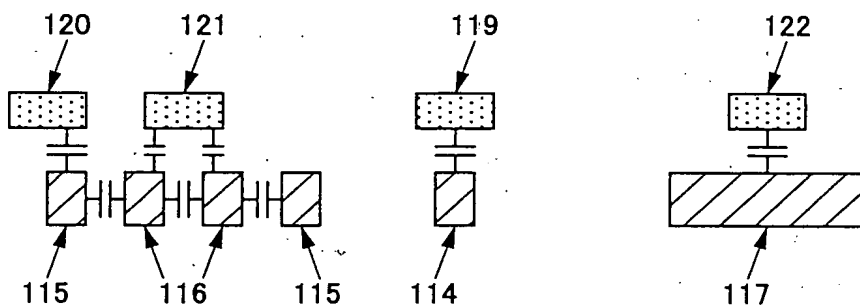


FIG.11

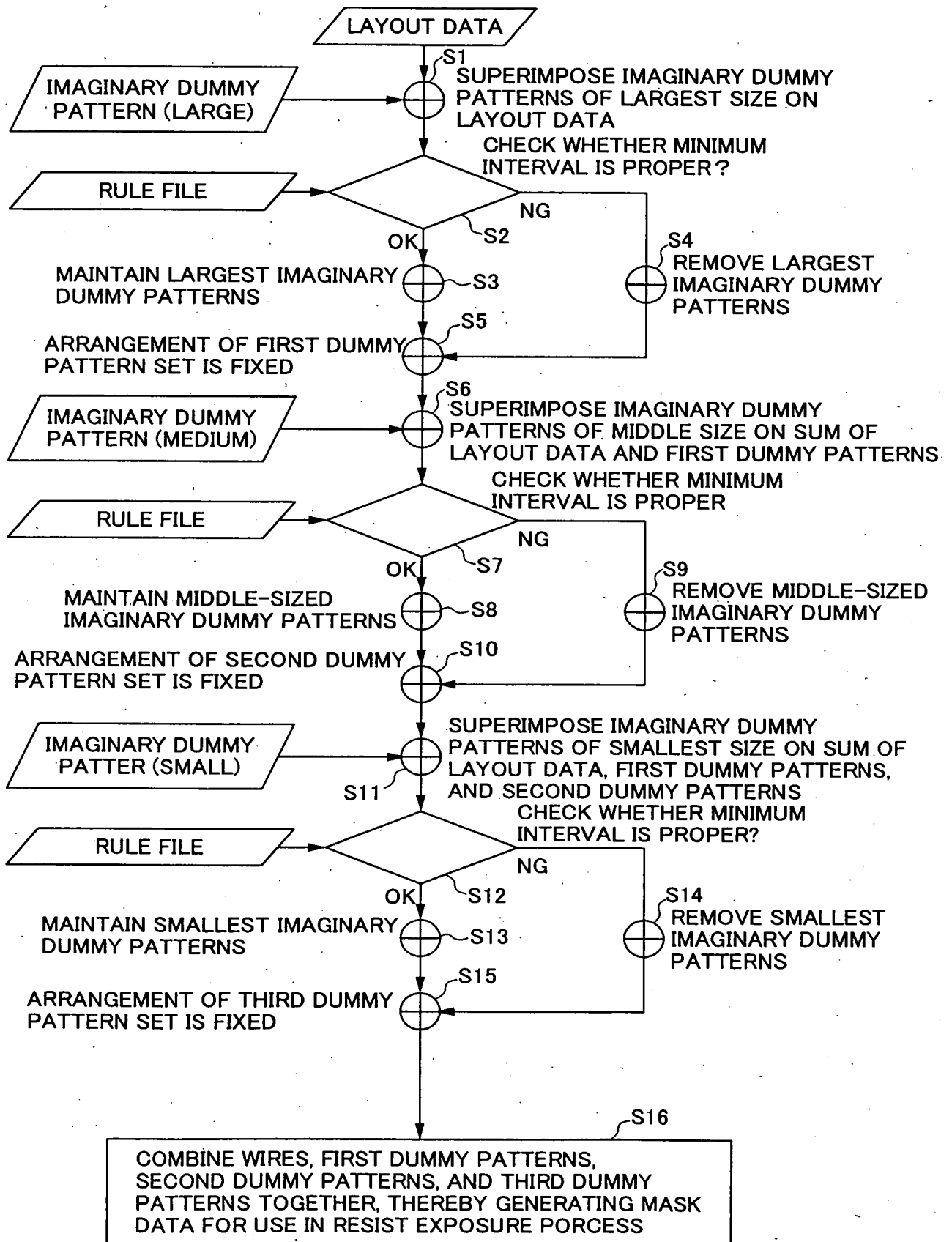


FIG. 11

FIG. 12A

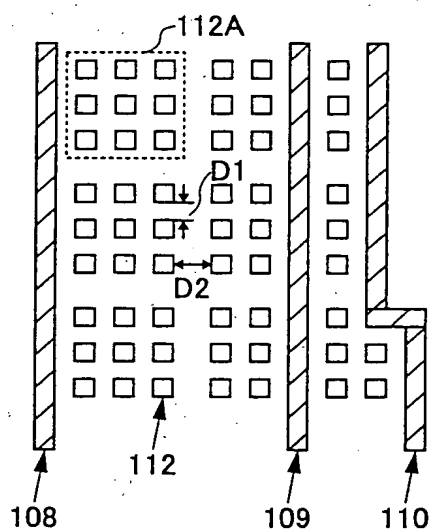


FIG. 12B

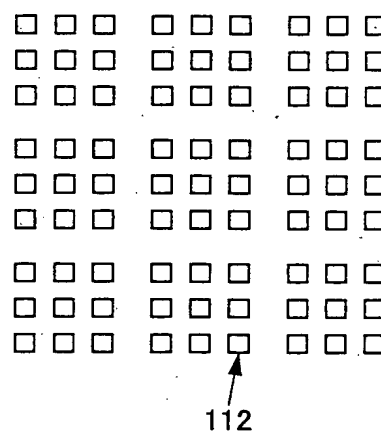


FIG. 12C

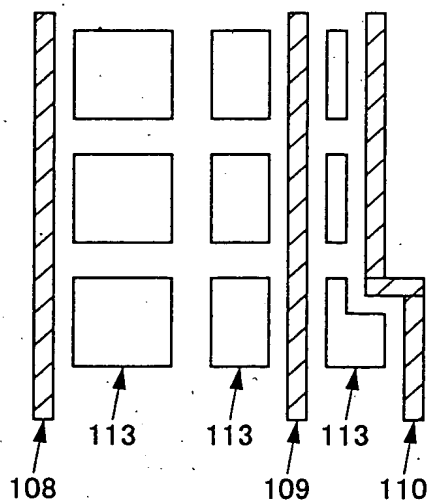


FIG.13

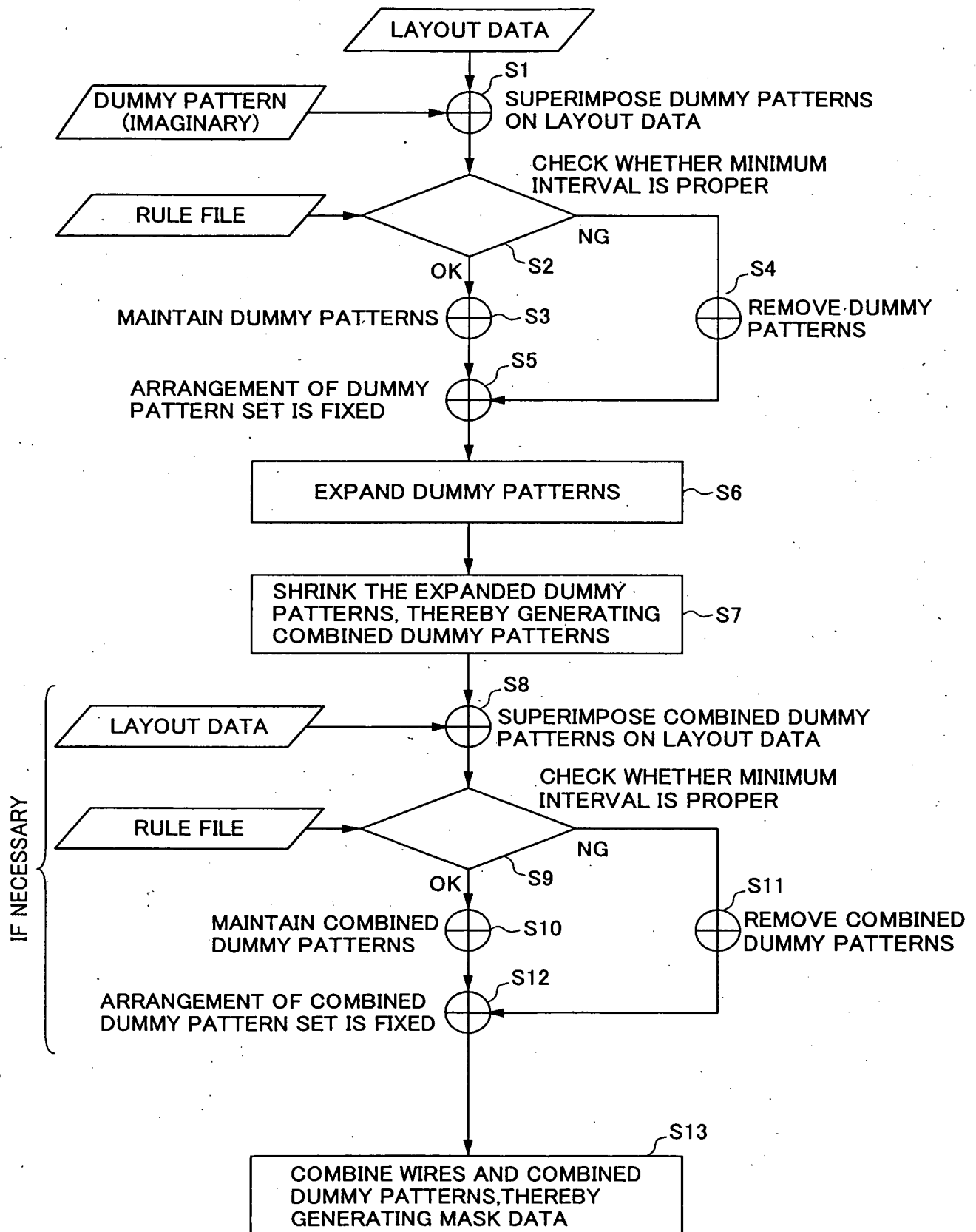


FIG.15

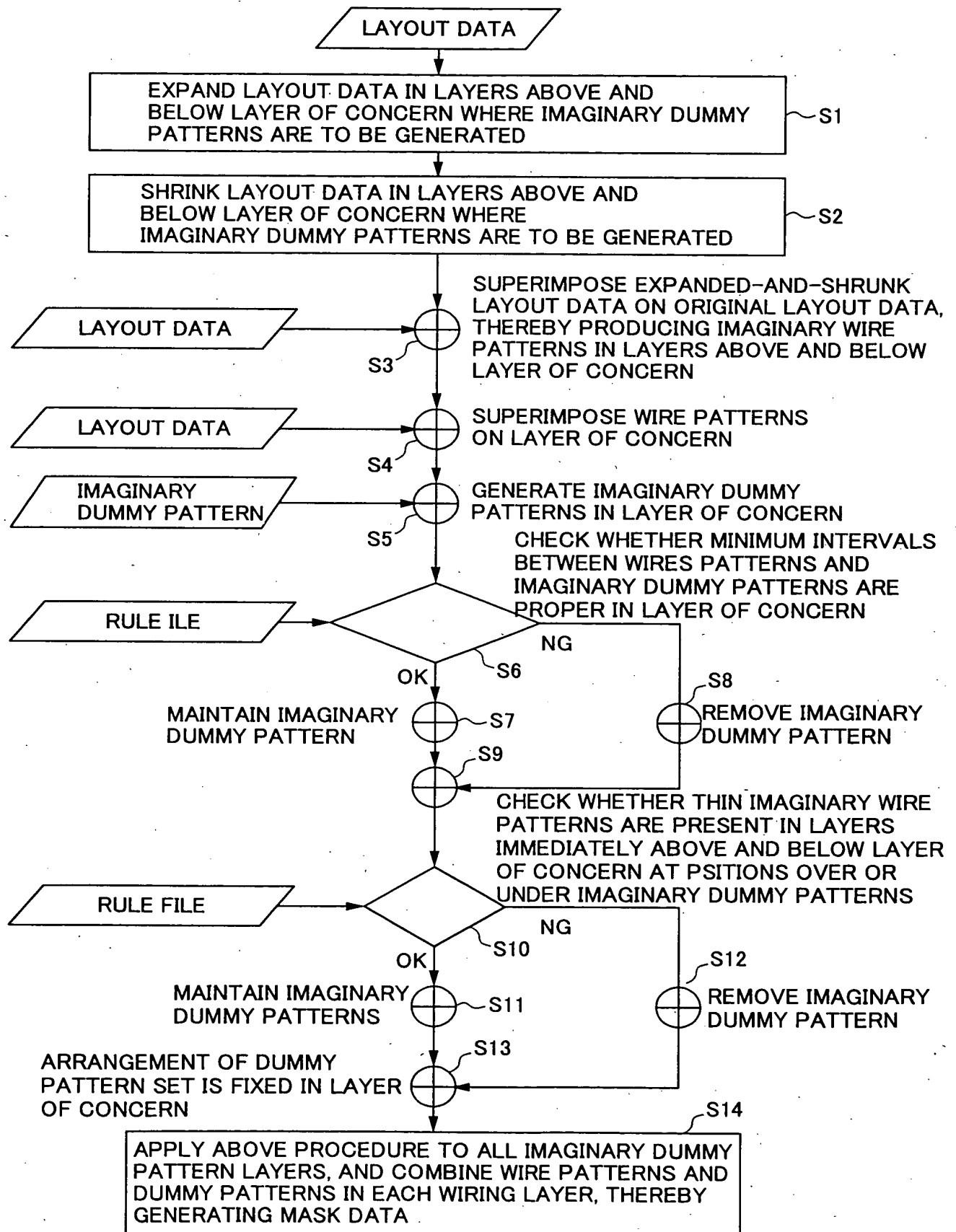


FIG. 16

INITIAL WIRES

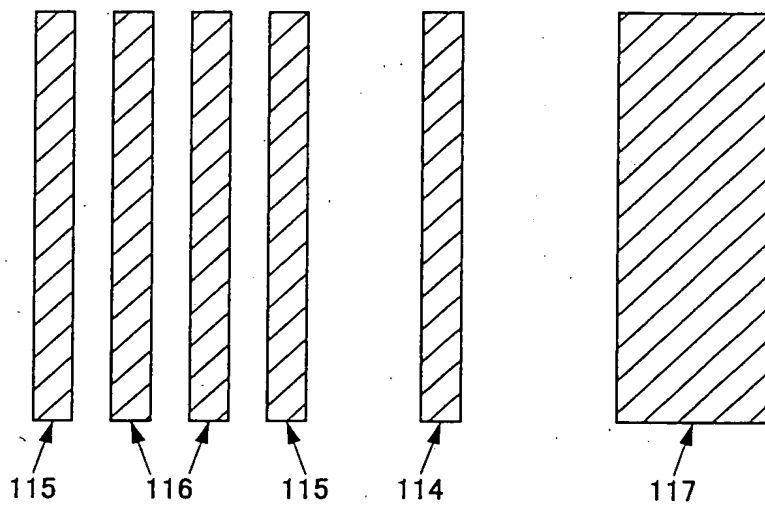


FIG. 17

FIRST PROCESS

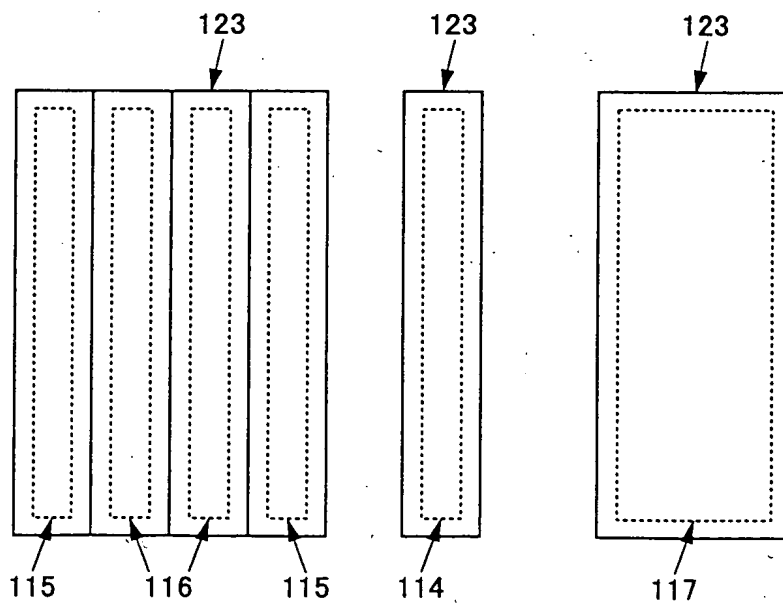


FIG. 18

SECOND PROCESS

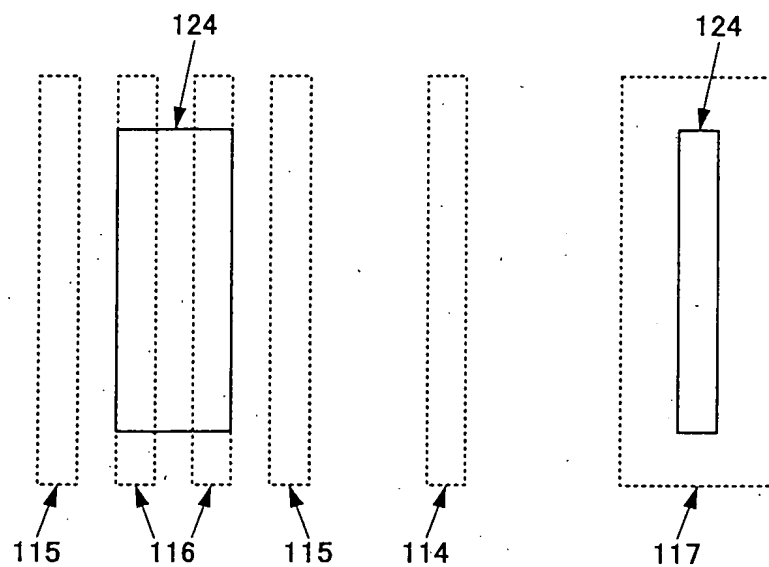


FIG. 19

THIRD PROCESS

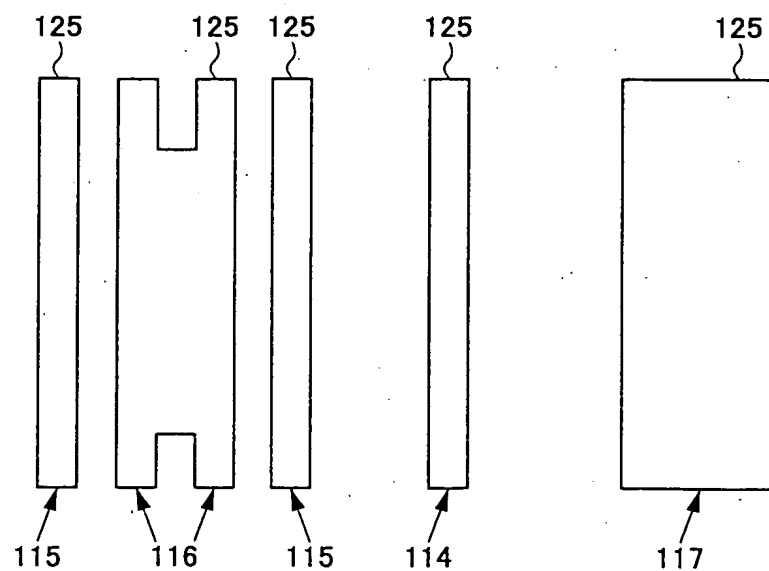


FIG. 20

FOURTH PROCESS

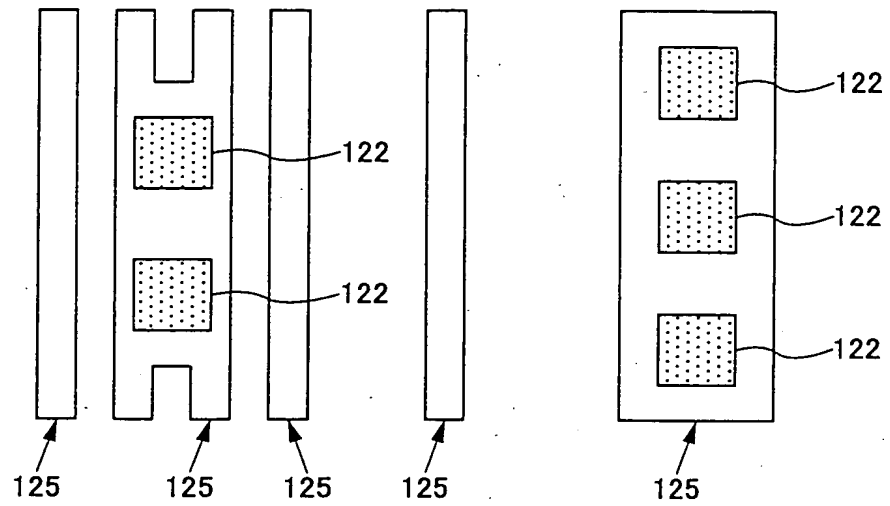


FIG. 21

FIFTH PROCESS

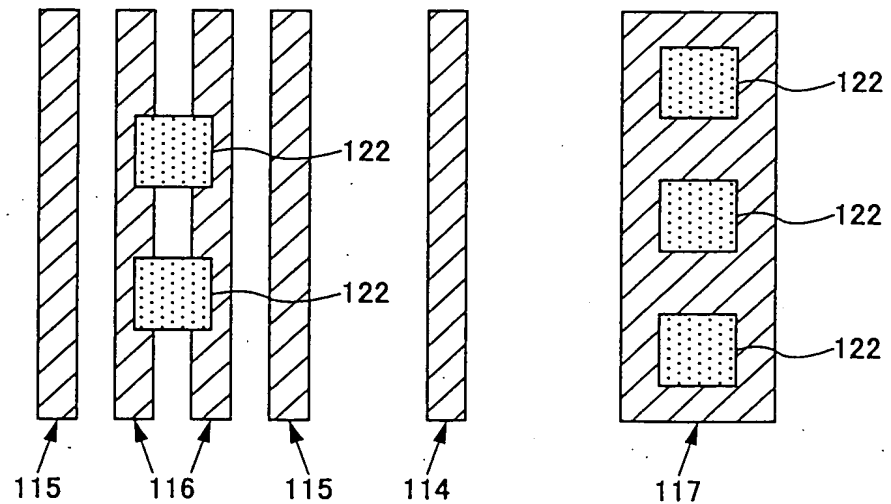


FIG. 22

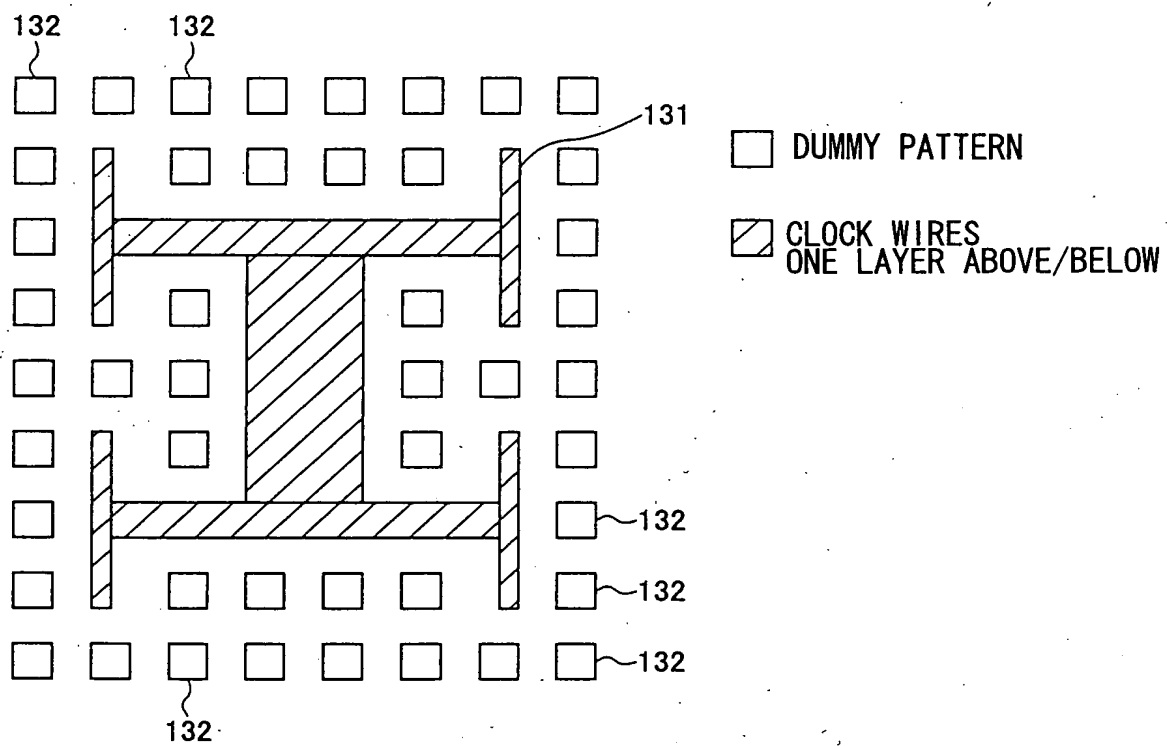


FIG.23

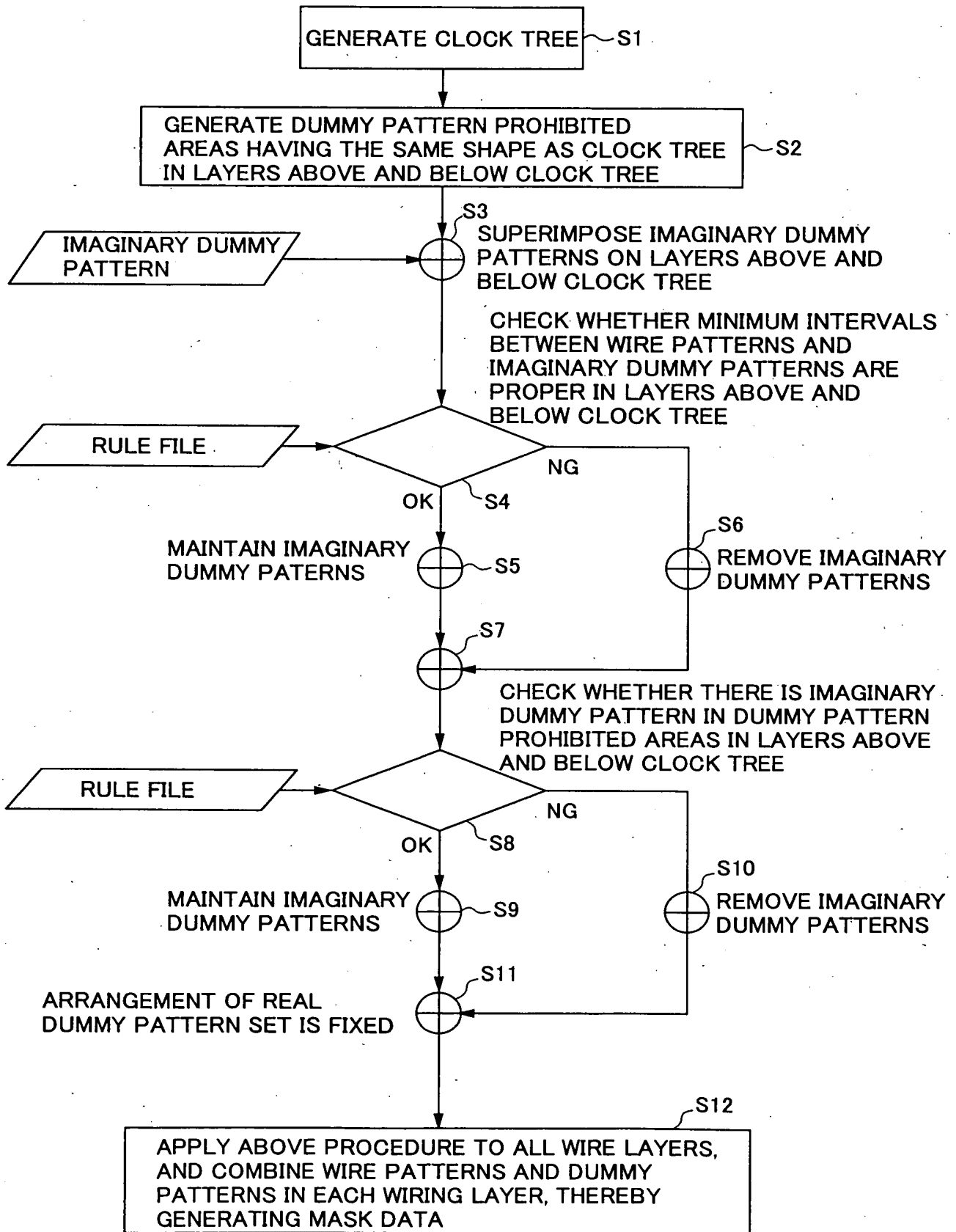


FIG. 24

